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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/040,727	12/28/2001	Stefan Johannes Bitterlich	9824-0077-999	2597

38881 7590 08/05/2005

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EXAMINER	
PHU, PHUONG M	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/040,727	BITTERLICH ET AL.	
	Examiner	Art Unit	
	Phuong Phu	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/17/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 36 and 37 are objected to because of the following informalities:

-In claim 36, it is unclear whether the limitation "a first processor core" refers to "a first processor core" recited in claim 33.

-In claim 37, the limitation "the second processor core" is lack of antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Subramanian et al (2002/0015401).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

-Regarding to claim 1, see figures 1A-1D, 2A-2F and 4, and sections [0032-0172], Subramanian et al discloses a channel CODEC processor (see figure 1B), comprising:

an algorithm-specific kernel block (104) operable to receive a data stream, the kernel block comprising logic tailored to perform at least one step of a channel CODEC algorithm on the data stream; and

a processor core (112, 121) coupled to provide configuration data to the algorithm-specific kernel block, the configuration data causing the kernel block to perform the at least one step of the channel CODEC algorithm according to one of a plurality of wireless communication standards as specified by the configuration data.

-Regarding to claim 2, Subramanian et al discloses an interconnect (126) through which data flows between the processor core and the algorithm-specific kernel block, wherein the processor core is operable to provide configuration data to the interconnect to control data-flow between the processor core and the algorithm-specific kernel block (see figure 1B).

-Regarding to claim 3, Subramanian et al discloses that the configuration data controls operation parameters of the algorithm-specific kernel block (see (11) of figure 1A, (121) of figure 1B), and [0034, 0037].

-Regarding to claim 4, Subramanian et al discloses the processor core is operable to perform time-multiplexed operations for a plurality of concurrent channel CODEC tasks (see [0037]).

-Regarding to claim 5, Subramanian et al discloses that the processor core is operable to perform another step of the channel CODEC algorithm (see [0037, 0039, 0040]).

-Regarding to claim 6, Subramanian et al discloses that the processor core is operable to perform steps of another channel CODEC algorithm (see [0037, 0039, 0040]).

-Regarding to claim 7, Subramanian et al discloses a local memory (106, 118) coupled to the processor core (see figure 1B).

-Regarding to claim 8, Subramanian et al discloses a local memory (106, 118) coupled to the algorithm-specific kernel block (see figure 1B).

-Regarding to claims 9, 10, Subramanian et al discloses that the logic of the algorithm-specific kernel block is tailored to decode data in the data stream according to a Viterbi (convolutional) decoding algorithm (see (418) of figure 4, and [0155]).

-Regarding to claim 11, Subramanian et al discloses the logic of the algorithm-specific kernel block is tailored to decode data in the data stream according to a Turbo decoding algorithm (see (420) of figure 4, and [0155]).

-Regarding to claim 12, Subramanian et al discloses that the algorithm-specific kernel block comprises a reconfigurable encoder (406) for convolutional codes in which at least one polynomial parameter of the encoder is controlled by the configuration data (see figure 4, and [0158]).

-Regarding to claim 13, Subramanian et al discloses that the algorithm-specific kernel block comprises a reconfigurable encoder (406) for Turbo codes in which at least one polynomial parameter of the encoder is controlled by the configuration data (see figure 4, and [0158]).

-Regarding to claim 14, Subramanian et al discloses the algorithm-specific kernel block comprises a reconfigurable cyclic-redundancy check (CRC) encoder (inherently included in (406)) (see (406) and (422) of figure 4, and [0039, 0155, 0158]).

-Regarding to claim 15, Subramanian et al discloses that the algorithm-specific kernel block comprises a reconfigurable cyclic-redundancy check (CRC) checker (422) (see figure 4, and [0155]).

-Regarding to claim 16, see figures 1A-1D, 2A-2F and 4, and sections [0032-0172], Subramanian et al discloses a channel CODEC processor, comprising:

a first algorithm-specific kernel block (418) (see figure 4) operable to receive a data stream, the first algorithm-specific kernel block comprising logic tailored to perform a step of a first channel CODEC algorithm on the data stream to generate a first processed data stream;

a second algorithm-specific kernel block (422) (see figure 4) coupled to the first algorithm-specific kernel block to receive the first processed data stream, the second algorithm-specific kernel block comprising logic tailored to perform a step of a second channel CODEC algorithm on the first processed data stream to generate a second processed data stream; and

a processor core (112, 121) (see figure 1B) coupled to provide configuration data to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel CODEC algorithm and the step of the second channel CODEC algorithm according to one of a plurality of wireless communication standards as specified by the configuration data.

-Regarding to claim 17, Subramanian et al discloses an interconnect (126) (see figure 1B) through which data flows among the processor core and the algorithm-specific kernel blocks,

wherein the processor core is operable to provide configuration data to the interconnect to control data-flow among the processor core and the algorithm-specific kernel blocks.

-Regarding to claim 18, Subramanian et al discloses that a first configuration data (inherently included in (121)) controls operation parameters of the first algorithm-specific kernel block and a second configuration data (inherently included in (121)) controls operation parameters of the second algorithm-specific kernel block .

-Regarding to claim 19, Subramanian et al discloses that the processor core is operable to perform time-multiplexed operations for a plurality of concurrent channel CODEC tasks (see [0158]).

-Regarding to claim 20, Subramanian et al discloses that the processor core is operable to perform steps of the first channel CODEC algorithm and the second channel CODEC algorithm (see [0037, 0042]).

-Regarding to claim 21, Subramanian et al discloses that the processor core is operable to perform steps of a third channel CODEC algorithm (see (406) of figure 4).

-Regarding to claim 22, see figures 1A-1D, 2A-2F and 4, and sections [0032-0172], Subramanian et al discloses a channel CODEC processor, comprising:

an input (129, 128) (see figure 1B) operable to receive a data stream;

a plurality of processor cores including a first processor core (102a) and a second processor core (108) operable to process data in the data stream (see figure 1B); and

a plurality of algorithm-specific kernel blocks including a first algorithm-specific kernel block (410) and a second algorithm-specific kernel block (406) (see figure 4) coupled to the first processor core and the second processor core, respectively, wherein the first algorithm-

specific kernel block is operable to receive first data from the first processor core and to perform at least one step of a first channel CODEC algorithm on the first data, wherein the second algorithm-specific kernel block is operable to receive second data from the second processor core and to perform at least one step of a second channel CODEC algorithm on the second data.

-Regarding to claim 23, Subramanian et al discloses that operation parameters of the first algorithm-specific kernel block and the second algorithm-specific kernel block are user-configurable (see figure 1D).

-Regarding to claim 24, Subramanian et al discloses that at least (121, 112) (see figure 1B) as one of the processor cores is coupled to provide configuration data to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel CODEC algorithm and the step of the second channel CODEC algorithm according to one of a plurality of wireless communication standards as specified by the configuration data.

-Regarding to claim 25, Subramanian et al discloses an interconnect (126) (see figure 1B) through which data flows among the processor cores and the algorithm-specific kernel blocks, wherein at least (121, 112) (see figure 1B) as one of the processor cores is operable to provide configuration data to the interconnect to control data-flow between the processor cores and the algorithm-specific kernel blocks.

-Regarding to claim 26, Subramanian et al discloses the processor cores are operable to perform time-multiplexed operations for a plurality of concurrent channel CODEC tasks (see [0033, 0034, 0158]).

-Regarding to claim 27, Subramanian et al discloses memories (106, 118) (see figure 1B) coupled to the processor cores.

-Regarding to claim 28, Subramanian et al discloses comprising memories (106, 118) (see figure 1B) coupled to the algorithm-specific kernel blocks.

-Regarding to claim 29, see figures 1A-1D, 2A-2F and 4, and sections [0032-0172], Subramanian et al discloses a communication device, comprising:

an I/O interface (116) operable to couple to an antenna (120) (see figure 1B);

a modem device (102a, 102b) for modulating and demodulating data coupled to the I/O interface(see figure 1B); and

a channel CODEC processor (104) (see figure 1B) coupled to the modem device to receive demodulated data stream, the channel CODEC processor comprising:

a first algorithm-specific kernel block (410) (see figure 4) operable to receive the demodulated data stream, the kernel block comprising logic tailored to perform at least one step of a channel decoding algorithm on the demodulated data stream; and

a first processor core (121, 112) (see figure 1B) coupled to provide first configuration data to the algorithm-specific kernel block, the configuration data causing the kernel block to perform the at least one step of the channel decoding algorithm according to one of a plurality of wireless communication standards as specified by the first configuration data.

-Regarding to claim 30, Subramanian et al discloses that the first processor core is operable to perform steps of the channel decoding algorithm (see (418, 420, 422) of figure 4).

-Regarding to claim 31, Subramanian et al discloses a network interface (108) (see figure 1B) operable to receive a data stream from a network, and

wherein the channel CODEC processor further comprises:

a second algorithm-specific kernel block (406) (see figure 4) operable to receive the data stream, the kernel block comprising logic tailored to perform at least one step of a channel encoding algorithm on the data stream; and

a second processor core (121, 112) coupled to provide second configuration data to the algorithm-specific kernel block, the configuration data causing the kernel block to perform the at least one step of the channel encoding algorithm according to one of a plurality of wireless communication standards as specified by the second configuration data.

-Regarding to claim 32, Subramanian et al discloses that the second processor core is operable to perform steps of the channel decoding algorithm (see figures 1B and 4).

-Regarding to claim 33, see figures 1A-1D, 2A-2F and 4, and sections [0032-0172], Subramanian et al discloses a communication device, comprising:

an I/O interface (116) (see figure 1B) operable to couple to an antenna (120);

a modem device (102a, 102b) for modulating and demodulating data coupled to the I/O interface; and

a channel CODEC processor (104) coupled to the modem device to receive a demodulated data stream, the channel CODEC processor comprising:

a first algorithm-specific kernel block (418) (see figure 4) operable to receive the demodulated data stream, the first algorithm-specific kernel block comprising logic tailored to perform a step of a first channel decoding algorithm on the demodulated data stream to generate a first processed data stream;

a second algorithm-specific kernel block (422) (see figure 4) coupled to the first algorithm-specific kernel block to receive the first processed data stream, the second algorithm-specific kernel block comprising logic tailored to perform a step of a second channel decoding algorithm on the first processed data stream to generate a second processed data stream; and

a first processor core (121, 112) (see figure 1B) coupled to provide first configuration data to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel decoding algorithm and the step of the second channel decoding algorithm according to one of a plurality of wireless communication standards as specified by the first configuration data.

-Regarding to claim 34, Subramanian et al discloses that the first processor core is operable to perform steps of the channel decoding algorithms (see (418, 422) of figure 4).

-Regarding to claim 35, Subramanian et al discloses a network interface (108) (see figure 1B) operable to receive a data stream from a network.

-Regarding to claim 36, Subramanian et al discloses that the channel CODEC processor further comprises:

a third algorithm-specific kernel block (for code polynomial (R,K) operable to receive the data stream from the network interface, the third algorithm-specific kernel block comprising logic tailored to perform a step of a first channel encoding algorithm (for code polynomial (R,K) on the data stream to generate a third processed data stream (see [0158]);

a fourth algorithm-specific kernel block coupled to the third algorithm-specific kernel block to receive the third processed data stream, the fourth algorithm-specific kernel block comprising logic tailored to perform a step of a second channel encoding algorithm (puncturing

pattern) on the first processed data stream to generate a fourth processed data stream (see [0158]); and

a processor core (121, 118) (see figure 1B) coupled to provide second configuration data to the algorithm-specific kernel blocks, the configuration data causing the algorithm-specific kernel blocks to perform the step of the first channel encoding algorithm and the step of the second channel encoding algorithm according to one of a plurality of wireless communication standards as specified by the second configuration data.

-Regarding to claim 37, Subramanian et al discloses that the processor core (121, 118) is operable to perform steps of the channel encoding algorithms (see [0158]).

4. Claims 1-37 are rejected under 35 U.S.C. 102(e) as being anticipated by Subramanian et al (2002/0031166) (now referred as Subramanian et al II).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

Claims 1-37 are rejected, as being anticipated by Subramanian et al II, with the same reasons set forth for the respective claims, as being anticipated by Subramanian et al, set forth above (see Subramanian et al II, figures 1A-1D, 2A-2F and 4).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuong Phu whose telephone number is 571-272-3009. The examiner can normally be reached on M-F (6:30-2:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phuong Phu
Primary Examiner
Art Unit 2631

Phuong Phu

PHUONG PHU
PRIMARY EXAMINER

Phuong Phu
06/24/05